AN APPLICATION OF MEMBRANE PROBES FOR ON-WAFER TESTING OF UNMATCHED HIGH POWER MMICS

D. Tonks, W. Vaillancourt, K. Smith* and E. Strid*

Raytheon, Adv. Dev. Ctr., Andover, MA *Cascade Microtech Inc., Beaverton, OR

Abstract

A membrane probe capable of determining large signal power handling capabilities of discrete and partially matched large periphery FETs at microwave frequencies has been developed. This paper describes the application and implementation of a membrane probe for a 15.7 mm partially matched 6W power amplifier MMIC that employs off-chip matching networks for a high volume multichip module application.

Introduction

One of the keys to successful high volume production of microwave multichip modules (MCM) is using known good MMICs. The use of conventional on-wafer RF probing as a die screen has reduced first pass yield fallout of MCMs due to MMIC component failures to less than 3%. Performing on-wafer RF probing of MMIC die prior to module assembly is critical to achieving high yielding, low cost modules. For MMICs designed in a 50Ω system, on-wafer RF testing is easily accomplished using 50Ω coplanar probes. In the case of discrete FETs to be used for modeling information, it is customary to choose devices with peripheries of about 1.0 mm because the optimum load impedance is approximately 50Ω. For such devices, a good indication of power capabilities is obtained using conventional probes and a slide screw tuner. Prior to the development of the membrane probe technique reported here, the screening method for large signal power handling capabilities of large periphery, partially matched MMICs commonly consisted of a subassembly level build and test prior to module assembly. In applications such as communications systems, where large periphery devices are required, and efficiency requirements demand a low loss off-chip output matching network, a method for determining power handling capabilities of MMICs at wafer level is most valuable. Using conventional probes to evaluate large periphery devices has a number of disadvantages including potentially unstable operation. Even if stabilized, the RF performance using 50Ω probes cannot be used as a reliable indicator because too much loss is introduced through external tuning.

The membrane probe technique is useful for performing high power on-wafer tests for large periphery MMIC power amplifiers and discrete devices with non-50Ω interfaces.

Device Design and Requirements

A high efficiency (>60%) 6W, 1.6 GHz power amplifier combining a 15.7 mm partially matched GaAs FET amplifier with on-chip input matching and a low loss off-chip output matching was chosen for

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application of the membrane probe. This partially matched MMIC, already characterized for use in production, could be modified to accommodate the membrane-MMIC interface without degrading electrical performance or altering the footprint. After changing the thick metal MMIC fabrication mask to incorporate 4 mil square probe pads at interface points, a revised probeable partially matched MMIC was realized. The original and probeable versions of the chip are shown in Figure 1.

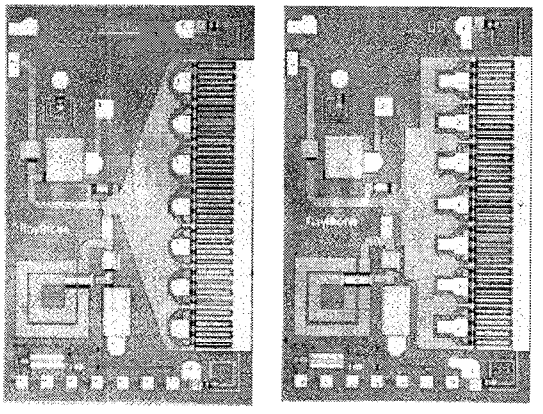

Figure 1. Both versions of MMIC

Implementation

The membrane and its printed circuit board together emulated the carrier board and module with respect to their interface with the MMIC. Once specifications were agreed between MMIC and membrane designers, the x-y coordinates of the MMIC pads were electronically transferred to membrane layout. A brief description of design elements follow: The carrier substrate is shown in Figure 2. An input signal was routed to the MMIC on a 50Ω microstrip line. The gate supply was bypassed on the carrier with a 100 pF capacitor. The carrier board provided a 2-section lumped element output matching network, which presented a load impedance of about 2.4Ω and approximately 7.5 pF. The drain current was supplied through a shunt inductive stub.

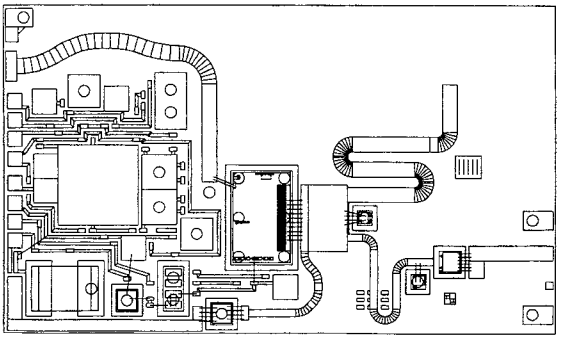

Figure 2. Carrier Substrate with MMIC Die

A schematic of the membrane is shown in Figure 3. A 50Ω line feeds the MMIC at the input interface. The gate bias pad was

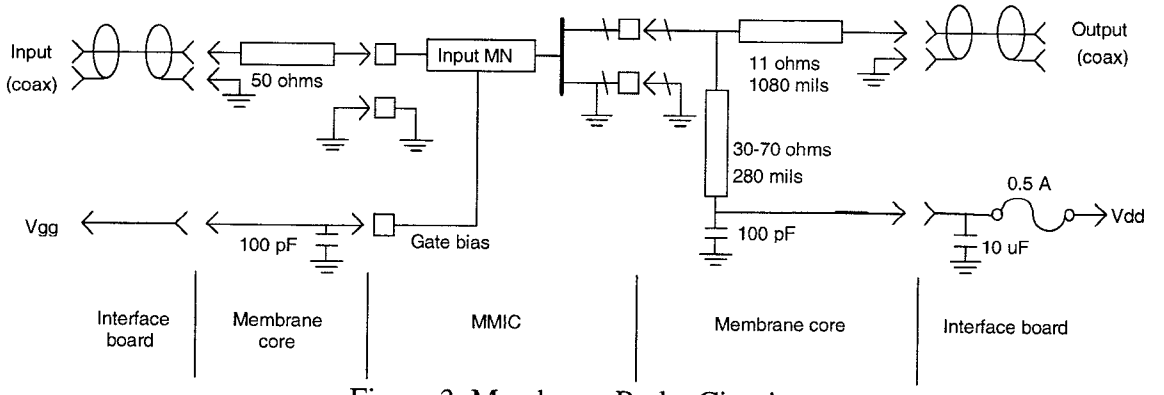

Figure 3. Membrane Probe Circuitry

bypassed with 100 pF using a 15Ω microstrip that was about 20 ps long. This 300 pH of series inductance duplicated the impedance of a bondwire connecting the capacitor on the substrate used in the module. On the membrane, the main element was the 11Ω quarter-wave line to match the 2.4Ω real part (at the open drain pads) to the 50Ω interface. This was laid out as two 22Ω lines in parallel, but could alternatively be produced by a single 11Ω microstrip line. The lines were adjusted to be slightly longer than 90° to achieve the imaginary part of the load impedance over the narrow bandwidth. (Other matching networks have used two or more quarterwave sections for larger bandwidths.) As seen in Figure 4 the 22Ω lines were implemented as a solid signal conductor over the meshed ground plane. In such a construction, the delay and loss are determined by the ground mesh rather than by the signal conductors[1].

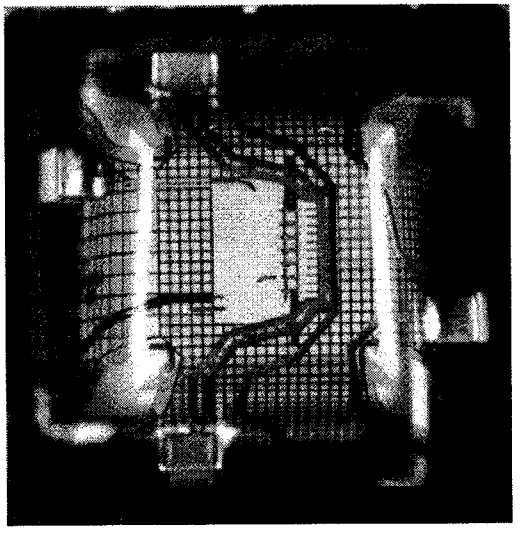

Figure 4. The Pyramid Probe

The drain bias was supplied by a short (<30°) transmission line connected to a 100 pF bypass capacitor. This is similar to the bias injection network used on the module carrier circuit board.

Membrane Probe Construction

The Pyramid Probe™ design allows the membrane to leave the wafer surface at a "high angle of attack". Matching networks are designed to start the impedance transformation immediately adjacent to the bond pads. The high angle of attack reduces the coupling between signal lines on the membrane and structures on the wafer.

The membrane incorporates a 20 um thick polyimide dielectric between 4 um thick copper conductors. The nickel alloy contact bumps are 35 um tall. Signal lines range from 40 microns to 250 um wide. Unlike standard coplanar probes which are often difficult to align[2], the membrane is nearly transparent and easily aligns to the MMIC pads.

Test Considerations

In order to eliminate heating effects the measurements were performed using a 1 ms pulsed, single tone signal with 10% duty cycle. Performing pulsed tests also reduced average current by a factor of ten and protected the probe from damage.

A response calibration was performed using a custom standard for the membrane probe thru. A slightly lifted membrane was used for an open circuit reference. The "impedance standard" for the thru was customized to fit the membrane pad locations. The total thru loss was 4.0 dB of which .75 dB was attributed to the input losses and 3.25 dB to output losses.

™ Pyramid Probe is a trademark of CMI.

Results

For the sample of measured devices, the power output capabilities were consistent over the wafer using the fixed load environment. Stability did not present any problems. As can be seen in Figure 5, at backed-off power levels gain varied as a function of bias point, however saturated power levels of 6W were repeatably measured using the membrane.

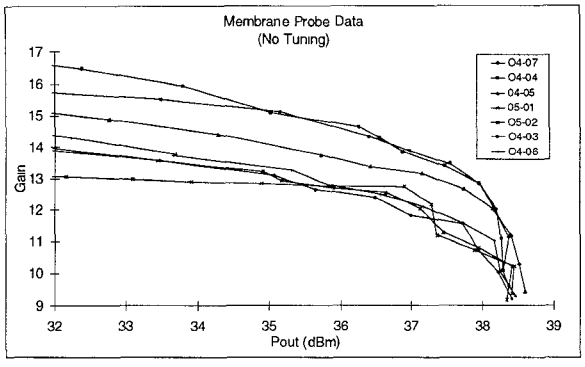

Figure 5. Gain vs. Output Power plotted for seven MMIC chips measured using the membrane probe.

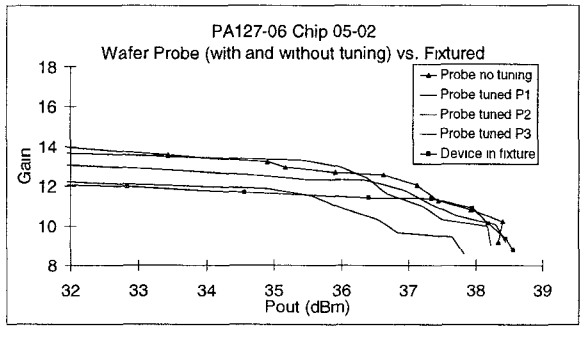

Figure 6. Data comparing fixtured carrier and membrane results for a MMIC where membrane is tuned externally.

In general, external tuning can be used in conjunction with the membrane once a close estimate of loadline is established. As shown in Figure 6, we were able to experimentally demonstrate our ability to manipulate the membrane probe match to the desired match using minimal external tuning. The ability to select a fixed output match for production testing was realized.

Concluding Remarks

In applications where high efficiency high power MMIC amplifiers are required, output matching networks must often be moved off-chip to meet cost and performance goals. Conventional 50Ω probe technology can not be used to accurately measure the performance of these un-matched low impedance devices at the wafer level even when combined with external tuning. By using the membrane probe we were able to locate the desired matching circuit on the RF probe and measure at power levels representative of our module application. Membrane probe technology, along with minor layout changes to make the device probeable, enabled us to perform an accurate and repeatable RF screen of large periphery, partially matched die on-wafer.

References

1 C-P Chien, M. Tanielian, J. Cech and A. Burnett. "The High Clock Rate Digital Signal Propagation Characteristics of Microstrip Interconnects Over a Perforated Reference Plane in Copper/Polyimide MCMs" in The International Journal of Microcircuits and Electronic Packaging, Vol 18, No 3, 3rd Quarter 1995

2 Goyal, R, Monolithic Microwave Integrated Chips, Technology and Design Artech House 1989.